# Hanyu WANG

(+41)79-222-6346
[hanywang@student.ethz.ch](mailto:hanywang@student.ethz.ch)
Gertrudstrasse 84
8003 Zurich, Switzerland

## EDUCATION

| | |
|---|---|
| 09/2021 - present | **Master of Science**, Electrical Engineering Information Technology<br>Swiss Federal Institute of Technology Zurich<br>**GPA**: Core: 5.82/6.00, All: 5.53/6.00 |
| 09/2017 - 08/2021 | **Bachelor of Engineering**, Electrical and Computer Engineering<br>University of Michigan-Shanghai Jiao Tong University Joint Institute<br>**GPA**: 3.79/4.00 Ranking: 4/148 |

## EXPERIENCE

| | |
|---|---|
| 10/2022 - 06/2023 | **Research Intern**, DYNAMO Research Group<br>ETH, Zurich, Switzerland<br>Advisor: Prof. Lana Josipović |
| 10/2021 - 09/2022 | **Research Intern**, Integrated Systems Laboratory<br>EPFL, Lausanne, Switzerland<br>Advisor: Prof. Giovanni De Micheli |
| 06/2019 - 09/2021 | **Research Intern**, Emerging Computing Technology Laboratory<br>Shanghai Jiao Tong University, Shanghai, China<br>Advisor: Prof. Weikang Qian |
| 05/2020 - 11/2020 | **Research Intern (Remote)**, Computer Systems Laboratory<br>Cornell University, Ithaca, USA<br>Advisor: Prof. Zhiru Zhang |
| 01/2020 - 05/2020 | **Exchange Student**, Electrical and Computer Engineering<br>University of Wisconsin Madison, Wisconsin, USA<br>GPA: 4.00/4.00 |
| 12/2018 - 02/2019 | **Exchange Student**, German Language Program<br>Technical University of Berlin, Berlin, Germany |

## TEACHING

| | |
|---|---|
| 06/2023 - 08/2023 | **Teaching Assistant**, VLSI 4: Measurement and testing of VLSI Circuits<br>Supervised a student project that runs Scan Chain Implemented Fault<br>Injection using a 93000 tester. |
| 02/2023 - 06/2023 | **Teaching Assistant**, VLSI 2: Backend design, ETH Zurich<br>Assisted 12 exercises, including DFT in Synopsys DC, Floorplanning<br>and PnR in Cadence Innovus, and DRC LVS using Mentor Calibre. |
| 09/2022 - 12/2022 | **Teaching Assistant**, VLSI 1: HDL-based design for FPGAs, ETH Zurich<br>Assisted 8 exercises for HDL coding, FPGA deployment using Xilinx Vivado,<br>and High-level synthesis using Vivado HLS. |
| 05/2019 - 08/2019 | **Teaching Assistant**, VE475 Introduction to Cryptography<br>University of Michigan-Shanghai Jiao Tong University Joint Institute |
| 09/2019 - 12/2019 | **Teaching Assistant**, VP260 Honors Physics II<br>University of Michigan-Shanghai Jiao Tong University Joint Institute |
| 05/2019 - 08/2019 | **Teaching Assistant**, VP160 Honors Physics I<br>University of Michigan-Shanghai Jiao Tong University Joint Institute |

# SELECTED PROJECTS

| | |
|---|---|
| 06/2023 - 09/2023 | **Quantum State Preparation using an Exact CNOT Synthesis Formulation** |
| | ETH, Zurich, Switzerland |
| | ● Formulated quantum state preparation as a shortest path problem. |
| | ● Improved the CNOT consumption to prepare both symmetric and asymmetric quantum states by 30%. |
| 10/2022 - 06/2023 | **Simultaneous Technology Mapping and Buffer Insertion for HLS Performance Optimization** |
| | ETH, Zurich, Switzerland |
| | ● Formulated technology mapping and buffer insertion jointly in a MILP problem. |
| | ● Improved the performance of HLS with 11% area reduction and 13% execution time reduction. |
| 03/2022 - 07/2022 | **Minimum Circuit Size Problem Solver** |
| | EPFL, Lausanne, Switzerland |
| | ● Synthesized multi-output completely specified functions. |
| | ● Won 1st place in the global contest. |
| 05/2022 - 07/2022 | **Scan Chain Implemented Fault Injection,** VLSI4 Project |
| | ETH, Zurich, Switzerland |
| | ● Implemented SCIFI on hp93000 tester. |
| | ● Ran fault injection test on Pony. |
| 04/2021 - 09/2021 | **AIG Size Optimization using Simulated Annealing** |
| | Emerging Computing Technology Laboratory, Shanghai, China |
| | ● Implemented simulated annealing framework based on ABC rewriting, refactoring, and resubstitution. |
| | ● Reduced the area by 22% compared to the state-of-the-art logic synthesis command compress2rs in ABC. |
| 01/2021 - 03/2021 | **ReFO: Resubstitution-based Fanout Optimization for FPGA Delay Reduction** |
| | Huawei Inc, Shanghai, China |
| | ● Developed a resubstitution-based algorithm and reduced the total fanout on the critical path by 60% with a 5% area overhead. |
| 01/2020 - 04/2020 | **Global Router Competition**, ECE556 Project |
| | University of Wisconsin Madison, Wisconsin, USA |
| | ● Implemented Global Router with heterogeneous Rip-up Re-Routing |
| | ● Won 1st place in the 2020 contest with the lowest wire length. |

# HONORS & AWARD

| | |
|---|---|
| 07/2022 | **Competition**: 1st place in IWLS 2022 Contest |
| 11/2020 | **Scholarship**: Sam and Daisy Wu Research Scholarship (1 out of 162) |
| 11/2018 | **Scholarship**: Liming Yu Scholarship (6 out of 325) |
| 11/2018 | **Scholarship**: Undergraduate Excellence Scholarship |
| 09/2017 | **Scholarship**: John Wu & Jane Sun Excellence Scholarship |
| 11/2019 | **Competition**: Bronze Medal in the University Physics Competition |
| 11/2016 | **Competition**: 2nd Class Award in National Olympiad of Information (NOIP) |
| 09/2016 | **Competition**: 2nd Class Award in Chinese Physics Olympiad (CPhO) |

# LANGUAGE SKILLS

| | | |
|---|---|---|
| ● Chinese: | Native | |
| ● English: | GRE | 325 (V:155 Q:170 AW:4) |
| | TOEFL | 109 (R:30 L:25 S:27 W:27) |
| ● German: | Goethe A2 | |

# PUBLICATIONS

W: Workshop / C: Conference paper

C4. **H. Wang**, J. Cong, and G. De Micheli, *Quantum State Preparation Using an Exact CNOT Synthesis Formulation*, Design, Automation, and Test in Europe Conference (DATE), to appear, Mar. 2024.

C3. C. Meng, **H. Wang**, Y. Mai, W. Qian, and G. De Mechili, *VACSEM: Verifying Average Errors in Approximate Circuits Using Simulation-Enhanced Model Counting,* Design, Automation and Test in Europe Conference (DATE), to appear, Mar. 2024. **(Best Paper Nominee)**

C2. **H. Wang**, C. Rizzi, and L. Josipović, *MapBuf: Simultaneous Technology Mapping and Buffer Insertion for HLS Performance Optimization*, International Conference on Computer-Aided Design (ICCAD), to appear, Nov. 2023. **(Best Paper Nominee)**

W1. **H. Wang**, S. Lee, and G. De Micheli, *A Cost-generic Resubstitution Algorithm with Customizable Cost Functions*, International Workshop on Logic and Synthesis (IWLS), Jul. 2022.

C1. Y. Zhou, **H. Wang**, J. Yin, and Z. Zhang, *Distilling Arbitration Logic from Traces using Machine Learning: A Case Study on NoC*, Design Automation Conference (DAC), Dec. 2021. **(Best Paper Nominee)**